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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,062	07/22/2003	Suraj Singh	1020.P16540	8262
57035	7590	11/24/2006	EXAMINER	
KACVINSKY LLC C/O INTELLEVATE P.O. BOX 52050 MINNEAPOLIS, MN 55402			TRAN, KHAI	
			ART UNIT	PAPER NUMBER
			2611	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/625,062

Applicant(s)

SINGH, SURAJ

Examiner

KHAI TRAN

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 12/22/2003.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application
- ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ahn (US 2003/016393 A1).

Regarding claim 1, Ahn discloses an apparatus as shown in Figures 3, 4, 5, comprising: a timing error detector to detect a timing error (a timing error detecting part 301b) for symbol sampling, the timing error detector to detect an amount of timing error based upon a value of an intersymbol sample as compared to an average value of a plurality of symbol samples (In-phase (I), quadrature (Q) signals) (see [0017] illustrating that a timing error detecting part for obtaining two symbol sample from a signal from the filter and an intermediate sample thereof, and detecting information on a timing error from a result (a value) of multiplication of a difference of the two samples and the intermediate sample, a loop filter for providing a signal of a bandwidth according to a signal from the timing error detecting part, and an NCO for controlling a sampling timing of the re-sampling part in response to a signal from the loop filter); and see [0052], [0059], and [0060]).

Regarding claim 2, Ahn discloses that wherein the timing error detector is adapted to detect an amount of timing error based upon a value of an intersymbol sample minus an average value of plurality of symbol samples, the intersymbol located between at least two of the plurality of symbol samples (see [0058]).

Regarding claim 3, Ahn discloses that wherein the timing error detector is adapted to detect an amount of timing error based on an average of the values for first and second symbol samples minus a value of an intersymbol sample between the first and second symbol samples (see [0058]).

Regarding claim 4, Ahn discloses that wherein the first sample is a sample of first symbol, and the second sample is of a second symbol, the first and second symbol being successive symbols, and the intersymbol sample being a sample taken between the first and second symbol samples (assumes I and Q symbol samples).

Regarding claim 5, Ahn discloses that wherein the timing error detector is adapted to interpolate or estimate a value of the intersymbol sample based on one or more other sample values (see [0021]).

Regarding claim 6, Ahn discloses that wherein the timing error detector is adapted to measure the value of the intersymbol sample at a sampling point that is approximately mid-way between the first and second symbol samples (see Figure 7).

Regarding claims 7-8, Ahn discloses that the timing error detector is adapted to sign normalize the amount of timing error based on one or more of the signs of the first and second symbol samples (see [0063] illustrating that the multiplication of a difference signal between two symbol samples and an intermediate sample thereof, and extracting

Art Unit: 2611

a sign only from a result of the multiplication as a timing error, which permits to provide a very great average gain of the timing error, can shorten a time period required for capturing the timing error. Especially, since a very great gain can be obtained even in a case a 0 dB ghost is present, a timing offset can be captured within a short time period).

Regarding claim 9, Ahn discloses wherein the apparatus further comprises a demodulator (see [0035], a TV digital receiver comprises an antenna for receiving broadcasting signals). The demodulator is inherent in the TV digital receiver system.

Regarding claim 10, Ahn discloses the TV digital receiver. Therefore, a use of a transceiver is inherent in the TV digital receiver.

Regarding claim 11, Ahn discloses that the timing detector is adapted to first determine whether there has been a sign change, either positive to negative or negative to positive from the values of the first and second symbol samples before detecting the amount of timing error (see [0058]).

Regarding claim 12, Ahn discloses wherein the timing error is adapted to detect an amount of timing error for both in-phase (I) and quadrature (Q) signals (see [0047]).

Claims 13-14 are similar to claims 1 and 4. Ahn also discloses that the timing error detector adapted to detect an amount of timing error based upon at least a portion or half of a sum of the values for first and second symbol samples (see [0052] illustrating that the timing error can be obtained by using the I signal only, or as shown in FIG. 5 the timing error can be obtained by using both the I and Q signals. The first embodiment timing error detecting part in which only the I signal is used has a simple circuit system, and the second embodiment timing error detecting part in which only the

Art Unit: 2611

I and Q signals are used can provide a more accurate timing error, though a circuit system thereof is complicated as equivalent with at least a portion of a sum the values for the first and second symbol samples). Therefore, claims 13-14 are rejected under a similar rationale.

Regarding claim 15, Ahn discloses wherein the timing error detector is adapted to detect an amount of timing error for both in-phase (I) and quadrature (Q) signals (see [0047]).

Claim 16 is similar to claim 1. Ahn further discloses that the timing error detector adapted to determine whether there has been a sign change, either positive to negative or negative to positive, from the values of first and second symbol samples (see [0021]).

Claims 17-19 are similar to claims 5, 6, 9. Therefore, claims 17-19 are rejected under a similar rationale.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 20-43 rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 2003/0161393 A1) in view of Cannon (US 2006/0031275 A1).

Claims 20-22 are similar to claim 1. Ahn also discloses that the apparatus comprises an analog to digital (A/D) converter to convert an analog signal to a digital

Art Unit: 2611

signal (see Figure 3). Ahn fails to explicitly disclose at least one mixer coupled to the A/D converter provide digital data signals.

Cannon discloses a digital IF processing block including a mixer or mixers (18 as shown in Figure 1) connected to an A/D converter 11. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the mixer taught by Cannon into the teachings Ahn for mixing the digital signal output from the A/D converter in order to process IF carrier.

Regarding claim 23, Ahn discloses that wherein the timing error detector is adapted to detect an amount of timing error for both I and Q signals, the total timing error being based on the timing error for both I and Q signals (see [0052]).

Regarding claims 24-25, Ahn discloses that wherein the apparatus is adapted to apply a correction to the timing of symbol sampling is the amount of timing error exceeds a threshold; and to the timing of symbol sampling is the sum of the amount of timing errors for I and Q signal exceeds a threshold (see [0048] to [0052]).

Claim 26 is similar to claim 20, Ahn also discloses an equalizer coupled to an output of at least one mixer (a channel equalizing part 0035).

Regarding claim 29-31, the claims are similar to claims 1, and 10. Although, Ahn fails to explicitly disclose a processor coupled to the transceiver a memory, flash memory. However, these components are well known in the TV receiver ad taught by Ahn for storing and processing the digital signal.

Claims 32-37 are similar to claims 1-7. Therefore, claims 32 –37 are rejected under similar rationale.

Regarding claim 39, Ahn discloses adjusting the timing of the symbol sampling based on the amount of error (a timing error detecting part 301a, a loop filter 301, and an NCO 301d).

Claim 40 is similar to claim 24. Therefore, claim 40 is rejected under a similar rationale.

Claim 41 is similar to claims 1, 4, 6. Therefore, claim 41 is rejected under a similar rationale.

Claims 42-43 are similar to claims 1, 5, and 40. Therefore, claims 42-43 are rejected under a similar rationale.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kingston et al (U.S. Pat. 5,982,821) disclose a frequency discriminator.

Temerinac (U.S. Pat. 6,477,215) discloses a sampling control loop.

Boccuzzi et al (U.S. Pat. 6,731,697) disclose a symbol timing recovery method.

Kim (U.S. Pat. 6,986,080) discloses a timing error detector for digital signal receiver.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAI TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

Art Unit: 2611

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



KHAI TRAN
Primary Examiner
Art Unit 2611

KT
November 21, 2006